

# **MSI-P406**

## **PC/104 QUADRATURE DECODER/COUNTER CARD with Differential Inputs**

(Revised 06-18-2010)

***PC/104 Embedded  
Industrial Analog I/O Series***

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## I. DESCRIPTION

The MSI-P406 is a 32-bit quadrature decoder PC/104 card designed for monitoring up to 4 quadrature encoder inputs used in monitoring shaft positions and rotations for machine control and robotic applications. Differential inputs are RS-422 compliant on each channel and provide for operation in noisy industrial environments. Each channel provides a 32-bit binary up/down counter with selectable 1X, 2X or 4X decoding using an Agilent HCTL-2032 decoder IC. This device provides a digital noise filter network, decoding logic, a 32-bit counter, and a 32-bit latched output. In addition, the MSI-P406 provides index inputs for encoders that have indexing. A card outline is shown in Figure 1.

Inputs from quadrature encoders are applied to input connectors J1 thru J4 for differential quadrature signals A, B and Index inputs for each channel in use. Input signals are TTL levels. The clock employed for processing the input signals is selectable from SYSCLK (6 to 8.33 MHz, depending on the processor card

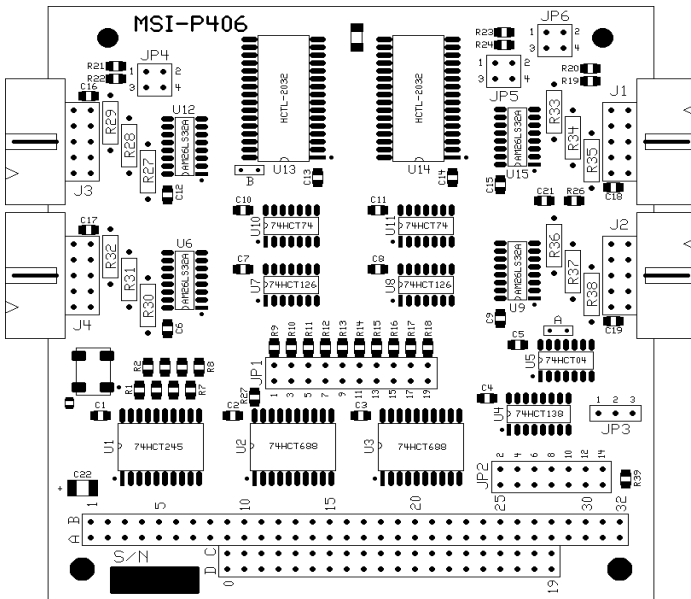


Figure 1. Outline of MSI-P406 Card.

used, or OSC at 14.318 MHz) of the PC/104 bus. As an option, clock oscillators from 2 to 33 MHz are available.

In addition to the quadrature inputs, +5V and GND connections are provided on the input connector for supplying power to the encoder of each channel. A shield ground that is connected to ground through a 0.1 uF capacitor is provided for shielded cables when these are used.

The maximum frequency that can be applied to either a frequency or reference input is

$$f_{\max} = \text{CLK}/7$$

Therefore, for CLK = 8.33 MHz,  $f_{\max} = 1.19$  MHz and for CLK = 14.318 MHz,  $f_{\max} = 2.045$  MHz.

Each channel has a 32-bit up/down counter and an output latch. When a frequency input (CHA\_x, x = 0 to 3) leads a reference input (CHB\_x, x = 0 to 3), nominally by 90 degrees, the counter counts up. Conversely, when the reference input leads the frequency input, nominally by 90 degrees, the counter counts down. Counts range from 0 to FFFFFFFF hexadecimal (0 to 4,294,967,295 decimal). Data reads require four Byte I/O reads to acquire the 32-bit count of each channel. Roll-over occurs for 0-to-FFFFFFF and FFFFFFFF-to-0 count transitions. These transitions are OR'ed together for use with interrupts IRQ3 thru IRQ9(2). The status of the roll-over channel is latched and can be read to determine the channel that is generating an interrupt when interrupts are employed. The interrupt latches are software resettable by reading the interrupt clear (INTCLR) port. The monitoring software must account for the roll-over events. A software reset is also provided for each channel that sets the count to 0. The card is an 16-bit stackthrough unit that requires +5V from the PC/104 bus.

An index input will reset the count for the channel to zero when an index pulse occurs if the channel is not disabled using option jumpers on JP4 and JP5.

## II. CARD CONFIGURATIONS

### A. Card Address Selection

The I/O-mapped card address is set by installing appropriate jumpers on JP1, pins 1 thru 19. An uninstalled jumper for a given address bit sets the bit to 0 (false) and an installed jumper sets the bit to 1 (true). Addresses A6 thru A15 are jumper selectable for defining the **base address** of the card from 0000H to FFC0H on integral 40H boundaries, where H denotes a hexadecimal number. To assign a base address of 300H, for example, install jumpers JP1-15,16 (A8) and JP1-13,14 (A9).

### B. Clock Source Selection

The clock source for the HCTL-2032 decoders is selectable by inserting the appropriate jumper on JP3 as follows:

JP3-1,2      PC/104 BUS SYCLK (Approx. 8 MHz)

JP3-2,3      PC/104 BUS OSC (14.318 MHz) \*

\* Factory Default setting.

Note: An optional clock from 1 to 33 MHz is available.

### C. Count Mode Selection

The HCTL-2032 decodes the incoming filtered signals into count information. This circuitry multiplies the resolution of the input signals by a factor of one, two or four (1X, 2X, 4X decoding) depending on the resolution mode. When using an encoder for motion sensing, the user benefits from the selectable resolution by being able to provide better system control. The quadrature decoder samples the outputs of the CHA and CHB filters. Based on the past binary state of the two signals and the present state, it outputs a count signal and a direction signal to the integral position counter. The 4x decoder mode

will output a count signal for every state transition (count up and count down). The 2x/1x decoder will output a count signal at respective state transition, depending on the counting direction. Channel A leading channel B results in counting up. Channel B leading channel A results in counting down.

The count mode for the HCTL-2032 decoders is selectable as 1X, 2X or 4X counting. Insert the appropriate jumpers on JP6 as follows:

None                    1X Decoding (Default)

JP6-1,3                2X Decoding

JP6-2,4                4X Decoding

#### **D. 32-Bit Counter Registers**

Four input channels, denoted as CH0 thru CH3, correspond to inputs CHA\_0 and CHB\_0 thru CHA\_3 and CHB\_3, respectively. The I/O addresses are given in Table 1. Total count data is obtained by performing four consecutive I/O reads at these addresses. The resulting channel count is

$$\text{Count} = \text{Low Byte} + 256 \times \text{2nd Byte} + 65,536 \times \text{3rd Byte} \\ + 16,777,216 \times \text{High Byte}$$

The channel counts can be read in any order and reading all registers is not required. For example, if only 16 bits is required for the application, only Low-Byte and 2nd-Byte counts need to be read. It is recommended that the registers be read from the highest count to the lowest count register for a given channel to help avoid missing a count during the read operation.

#### **E. Resetting the Counter Registers**

The counts contained in all registers (high to low bytes) can be reset to zero by performing an I/O read of the reset addresses

Table 1. Input Addresses of MSI-P406 Count Registers.

Channel	Low Byte of Count* 3rd Byte of Count*	2nd Byte of Count* High Byte of Count*
CH0	base address base address+2	base address + 1 base address + 3
CH1	base address+4 base address+6	base address + 5 base address + 7
CH2	base address+8 base address+AH	base address + 9 base address + BH
CH3	base address+CH base address+1EH	base address + DH base address + FH

\* *Offsets from the base address are in hexadecimal notation.*

of Table 2. This is a very useful function in many applications. At power-on, it is recommended that all channels be reset to zero performing a dummy **I/O read** to each reset channel address of Table 2.

Table 2. Reset Addresses of MSI-P406 Count Registers.

Channel	Reset Address *
CH0	base address + 10H
CH1	base address + 18H
CH2	base address + 20H
CH3	base address + 28H

\* *Offsets from the base address are in hexadecimal notation. Channels are reset by performing an I/O read at these addresses.*

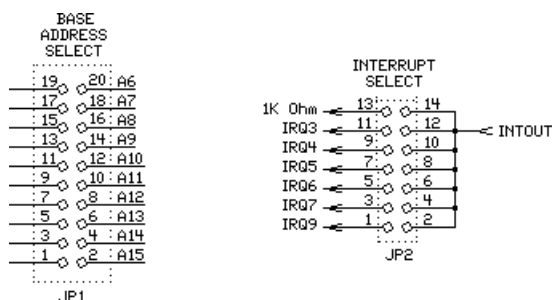


Figure 2. Base Address and Interrupt Jumper Selections.

## F. Interrupt (IRQ3 thru IRQ7, IRQ9) Selection

The HCTL-2032 decoders have 32-bit count registers and interrupt processing for rollover is usually not necessary. In cases where counts exceed 32 bits, interrupt processing for rollover can be used. Outputs RO-0 thru RO\_3 are OR'd together to generate a single interrupt signal in the event of an overflow or an underflow of any of the HTCL-2032 decoders. This signal is available on JP2 for jumper routing to the desired IRQx (where x = 3, 4, 5, 6, 7 or 9), as shown in Figure 2. When a rollover occurs, the interrupt is latched for each channel and remains valid until the latch is reset by performing an **I/O Byte read at base address + 38H**. Prior to resetting the latches, the status of the latches can be read at base address + 30H to determine the interrupting channel. This is normally performed in software by the user's interrupt handler. Bit positions of the status byte for the interrupting channel are given in Table 3.

A 1 KOhm pull-down resistor is jumper selectable on JP2, as shown in Figure 2, for use in avoiding a floating interrupt line when no interrupt request is present.

## G. Quadrature Input Connector Pin Assignments

The input connections for the quadrature inputs are provided by J1 thru J4. Also available are +5V and ground connections for powering the user's quadrature encoders. The pinouts for J1 thru J4 are given in Table 4 thru Table 7, respectively.

**Table 3. Interrupt Status Register of MSI-P406.**

Channel	Status Address *	Bit No.
CH0	base address + 30H	0
CH1	base address + 30H	1
CH2	base address + 30H	2
CH3	base address + 30H	3

\* Offsets from the base address are in hexadecimal notation.

**Table 4. Quadrature Input Connectors J1.**

Pin No.	Signal	Pin No.	Signal
1	CHA_0+	2	CHA_0-
3	CHB_0+	4	CHB_0-
5	CHI_0+	6	CHI_0-
7	GND	8	GND
9	SHIELD_GND	10	+5V

**Table 5. Quadrature Input Connectors J2.**

Pin No.	Signal	Pin No.	Signal
1	CHA_1+	2	CHA_1-
3	CHB_1+	4	CHB_1-
5	CHI_1+	6	CHI_1-
7	GND	8	GND
9	SHIELD_GND	10	+5V

Table 6. Quadrature Input Connectors J3.

Pin No.	Signal	Pin No.	Signal
1	CHA_2+	2	CHA_2-
3	CHB_2+	4	CHB_2-
5	CHI_2+	6	CHI_2-
7	GND	8	GND
9	SHIELD_GND	10	+5V

Table 7. Quadrature Input Connectors J4.

Pin No.	Signal	Pin No.	Signal
1	CHA_3+	2	CHA_3-
3	CHB_3+	4	CHB_3-
5	CHI_3+	6	CHI_3-
7	GND	8	GND
9	SHIELD_GND	10	+5V

## H. Enabling Index Inputs of the MSI-P406

Enabling the index inputs (CHI\_0 thru CHI\_3) are performed by placing the appropriate jumpers on JP4 and JP5, as shown in Table 8.

Table 8. Jumper Positions for Enabling Index Inputs.

Signal	Jumper	Enable	Disable
CHI_0	JP5-1,2	ON	OFF
CHI_1	JP5-3,4	ON	OFF
CHI_2	JP4-1,2	ON	OFF
CHI_3	JP4-3,4	ON	OFF

## I. Resistor Sites for Quadrature Input Line Matching

Resistor pads at sites R27 thru R38 are provided for 0.25W through-hole resistors for impedance matching, where required, for RS-422 compliant quadrature receiver lines of each channel. These sites permit the use of resistors matching the characteristic impedance of the cable connecting the inputs, usually twisted pairs with a nominal characteristic impedance of 100 Ohms. In high frequency applications, these resistors may be required. The SHIELD\_GND terminals provide a capacitive connection to the PC/104 BUS ground for connecting the cable shield when available. This has the advantage of isolating any dc component of the shield from the computer ground.

The resistor sites for the quadrature inputs for the four channels are given in Table 9.

Table 9. Resistor Sites for J1 thru J4.

Channel	Signal	Resistor Site
0	CHA_0+/-	R33
	CHB_0+/-	R34
	CHI_0+/-	R35
1	CHA_1+/-	R36
	CHB_1+/-	R37
	CHI_1+/-	R38
2	CHA_2+/-	R27
	CHB_2+/-	R28
	CHI_2+/-	R29
3	CHA_3+/-	R30
	CHB_3+/-	R31
	CHI_3+/-	R32

### III. SPECIFICATIONS

#### PC/104

16-bit, stackthrough

#### Quadrature Encoder and Index Inputs

Freq, Ref and Index (Quadrature inputs for each channel)

Meets or exceeds ANSI TIA/EIA-422-B

Max. Diff. Input Voltage +/-25V

#### Input Frequency

$$f_{\max} = \text{CLK}/7$$

$$f_{\max} = 1.19 \text{ MHz for CLK} = 8.33 \text{ MHz}$$

$$f_{\max} = 2.045 \text{ MHz for CLK} = 14.318 \text{ MHz}$$

#### Address Selection, Interrupt, Count Mode, and Clock Selection Jumpers (JP1 thru JP6)

Base Address Selection for A6 thru A15 (JP1)

Interrupts IRQ3 thru IRQ7 and IRQ9 (JP2)

Clock Selection SYSCLK or OSC of PC104 BUS (JP3)

Enable/Disable Index Inputs (JP4 & JP5)

Count Mode 1X, 2X, and 4X (JP6)

0.025" square posts, 0.1" grid

#### Input Connector (J1 thru J4)

Quadrature Inputs (Freq, Ref, Index, SHIELD\_GND)  
+5V and GND

3M 30310-5002 or equivalent.

#### Electrical & Environmental

+5V @ 250 mA typical

-40° to 85° C

#### Models

MSI-P406-2, 2 Channels

MSI-P406-4, 4 Channels

## **APPENDIX A**

### **MSI-P406 Circuit Diagram**

Schematic Diagrams of the MSI-P406

1) P406-1.sch - Schematic sheet 1 of 2.

**See p406-1.pdf**

2) P406-2.sch - Schematic sheet 2 of 2.

**See p406-2.pdf**

## **APPENDIX B**

### **HCTL-2032 Data Sheet**